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PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10082518	02/22/2002	326	16	2819	

**APPLICANTS: Hwang L.; Sanchez Reno;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		X-1002 US
Verified and Acknowledged Examiners's intials			

TITLE : Method and system for integrating cores in FPGA-based system-on-chip (SoC)

U.S.DEPT. OF COMM /PAT & TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING		
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.	Print Fig.
		Primary Examiner			
☐ TERMINAL DISCLAMER		PREPARED FOR ISSUE	Application Examiner		

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